

# VERSION HISTORY

4

3

2

1

## Index:

- 01 VERSION HISTORY
- 02 BLOCK DIAGRAM
- 03 POWER TREE
- 04 DDR3 16X2
- 05 CPU
- 06 PMIC
- 07 FLASH
- 08 AUDIO
- 09 USB/T-CARD
- 10 CAMREA
- 11 LCM/CTP
- 12 SENSORs/MT/KEY
- 13 HDMI
- 14 WIFI-BT
- 15 MODEM-2G

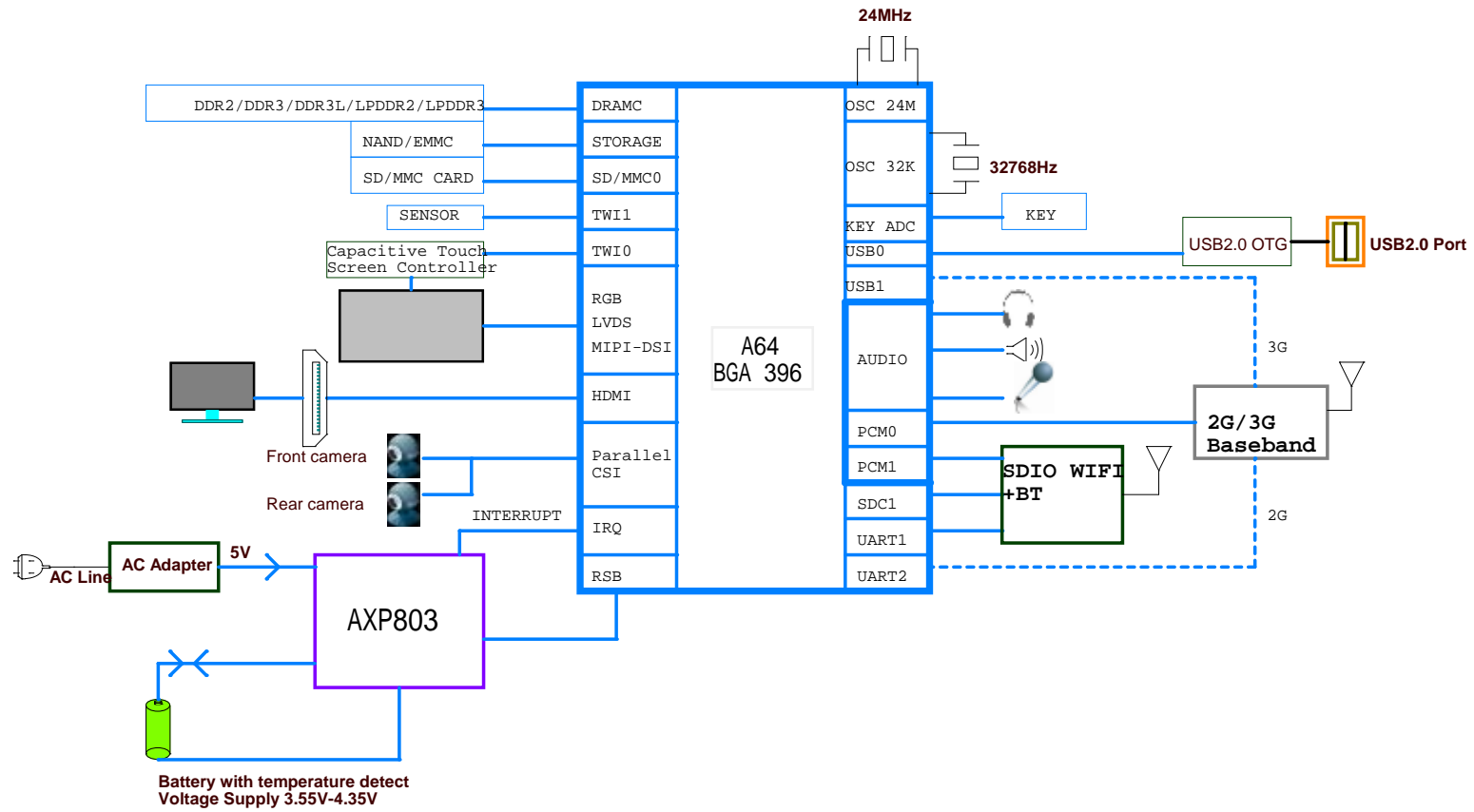
option

- 16 LPDDR3 FBGA178
- 17 LPDDR2/LPDDR3
- 18 MODEM-3G

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Releas version	2015-04-22			

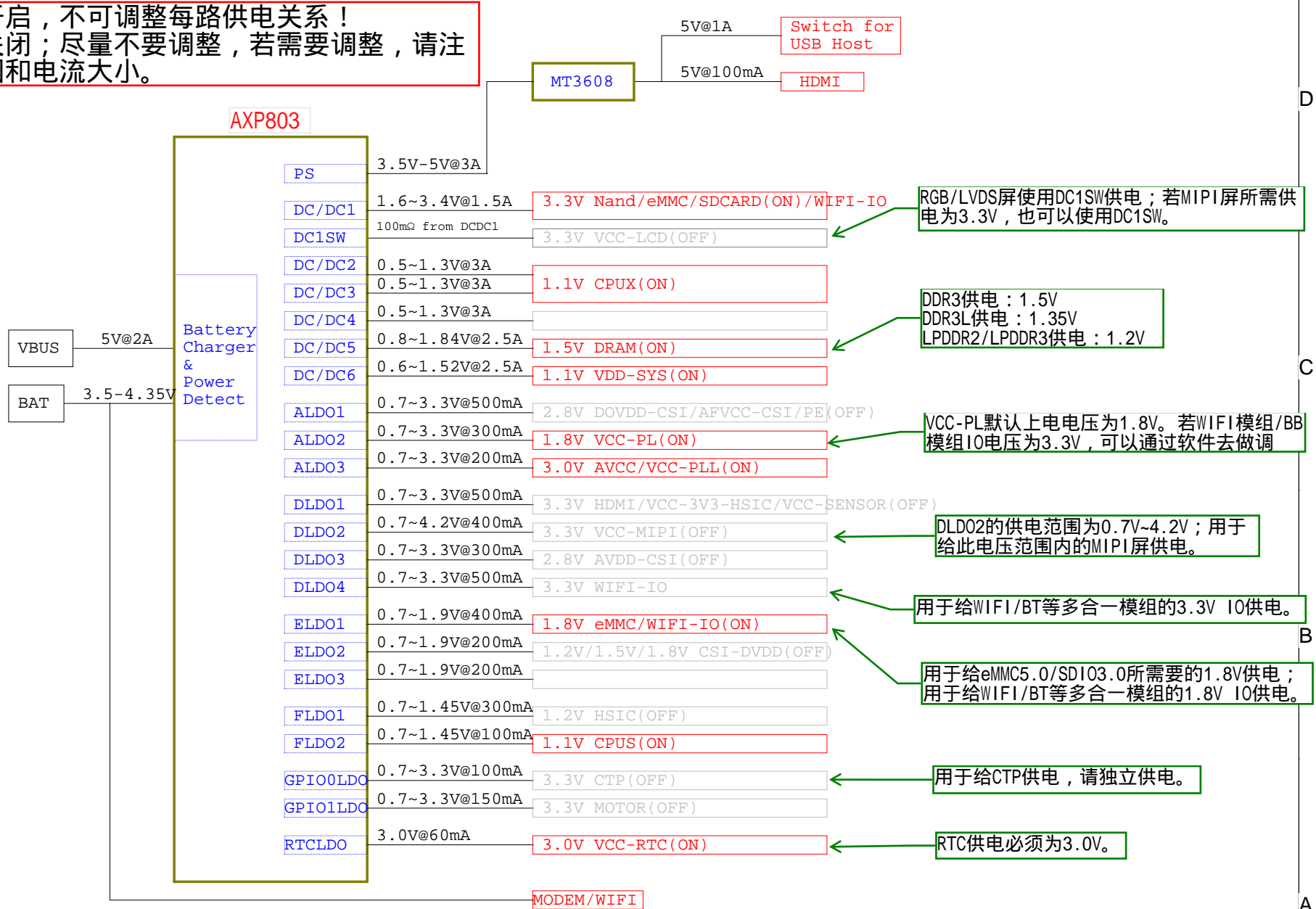
# 原理图设计说明V1.0

# BLOCK DIAGRAM



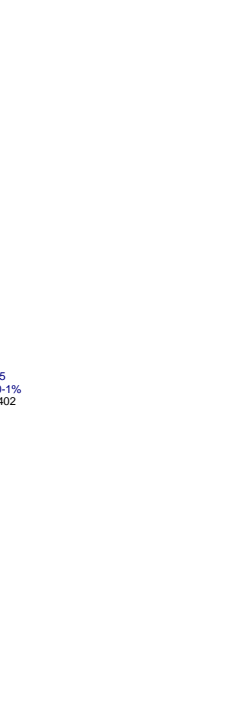
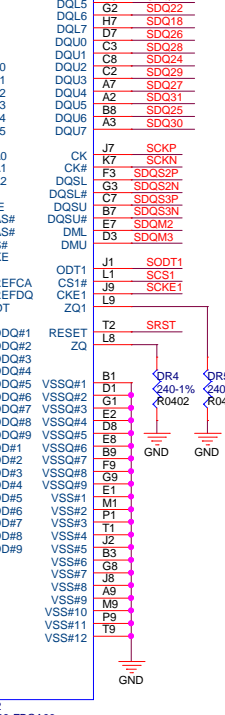
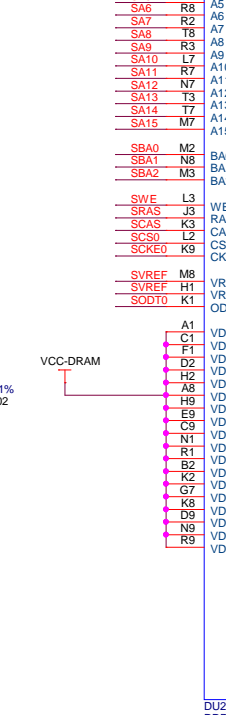
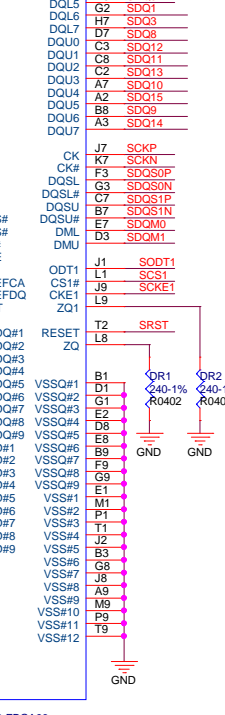
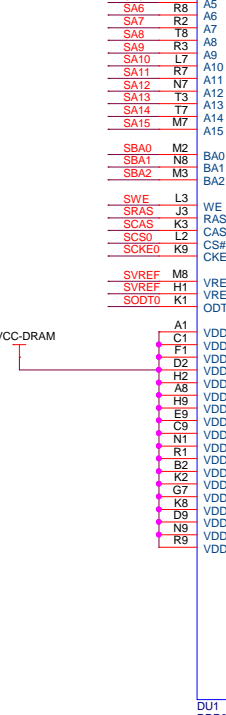
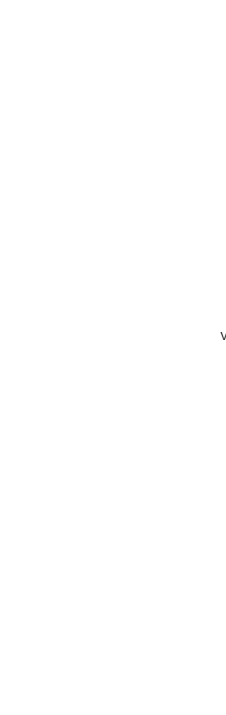
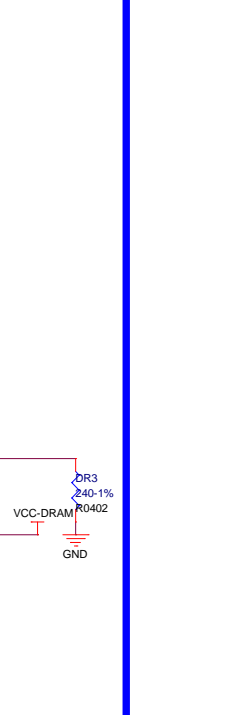
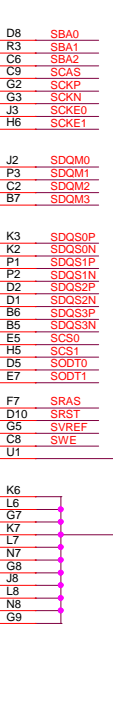
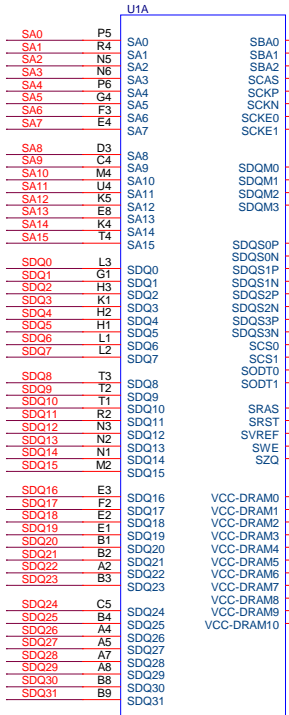
# POWER TREE

红色：上电默认开启，不可调整每路供电关系！  
 灰色：上电默认关闭；尽量不要调整，若需要调整，请注意每一路电压范围和电流大小。

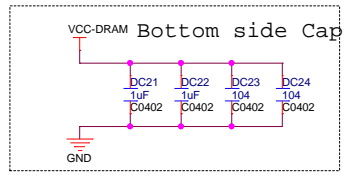
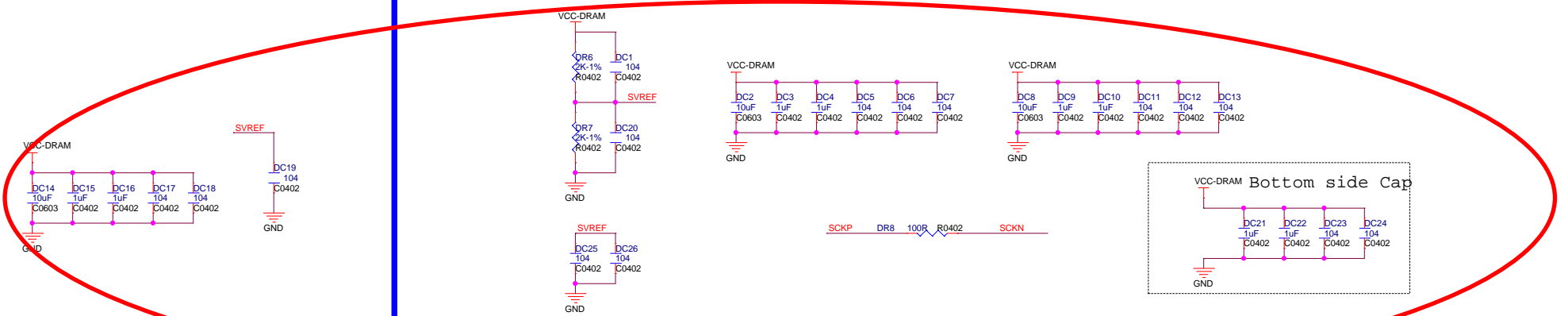


# DDR3 16x2

请尽量使用Allwinner提供的DDR Layout参考模板；否则请严格遵守DDR Layout Guide。



采用Allwinner DDR Layout模板，红色框中的元器件位号不能变。

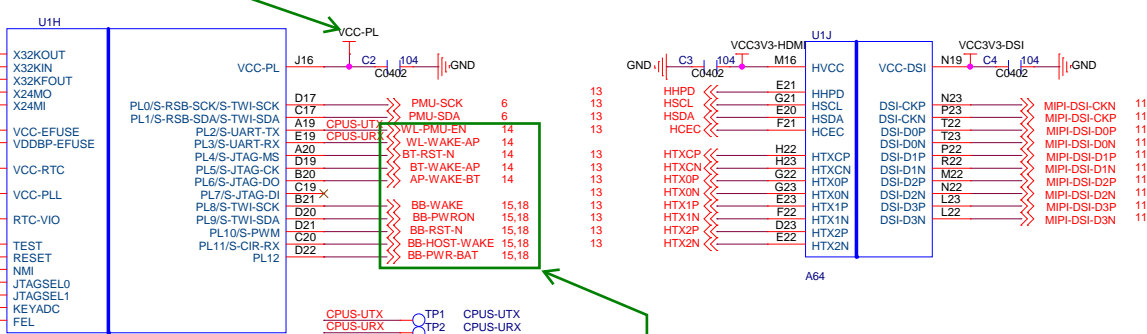


# CPU

VCC-PL的电压根据WIFI模组/BB基带的IO电压进行调整；默认为1.8V，可调整为3.3V。

EFUSE内部LDO输出电容，容值不可调整。

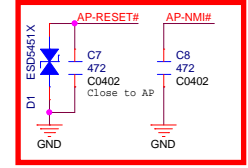
RTC内部LDO输出电容，容值不可调整。



远离板边及敏感信号，包地处理。

WIFI模组/BB基带的控制信号，控制关系尽量不要调整。

远离板边及敏感信号；最好能包地处理；走Power层。

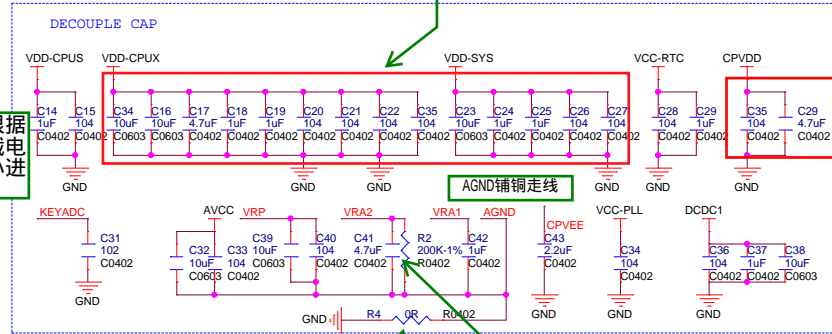
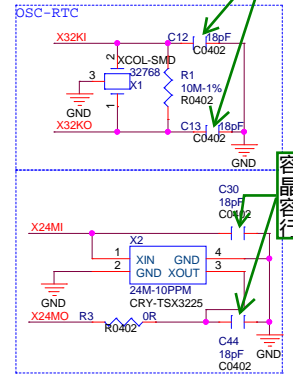


HPOUTL/HPOUTR走线宽度不小于8mil。

容值可根据晶体负载电容的大小进行调整！

为了保证系统的稳定性，电容的数量和容值大小尽量不要改动！

容值可根据晶体负载电容的大小进行调整！

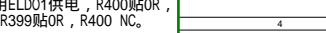
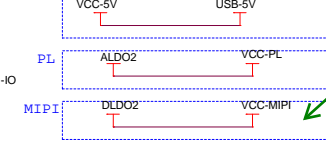
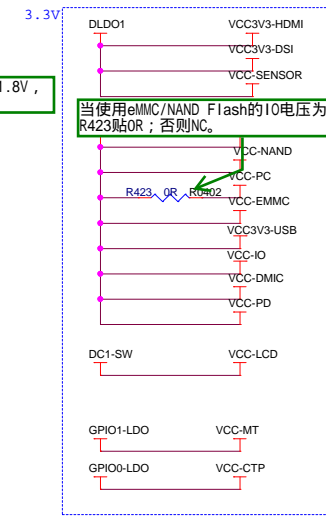
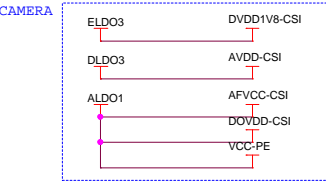
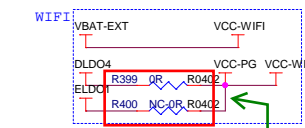
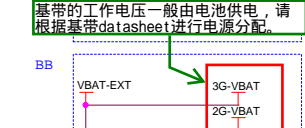
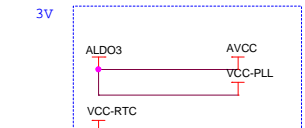
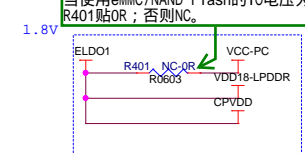
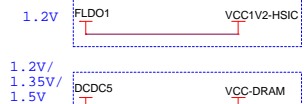
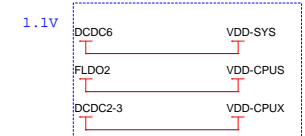
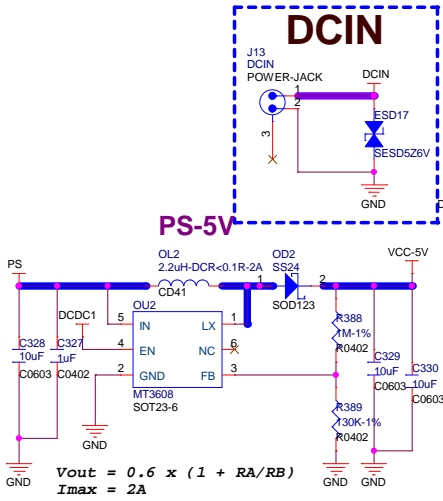
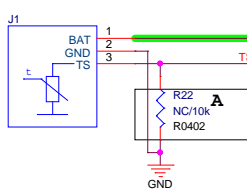


AGND与GND单点连接！

R2阻精度为1%，阻值不可调！

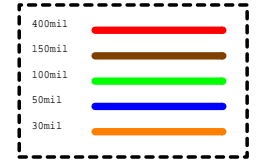
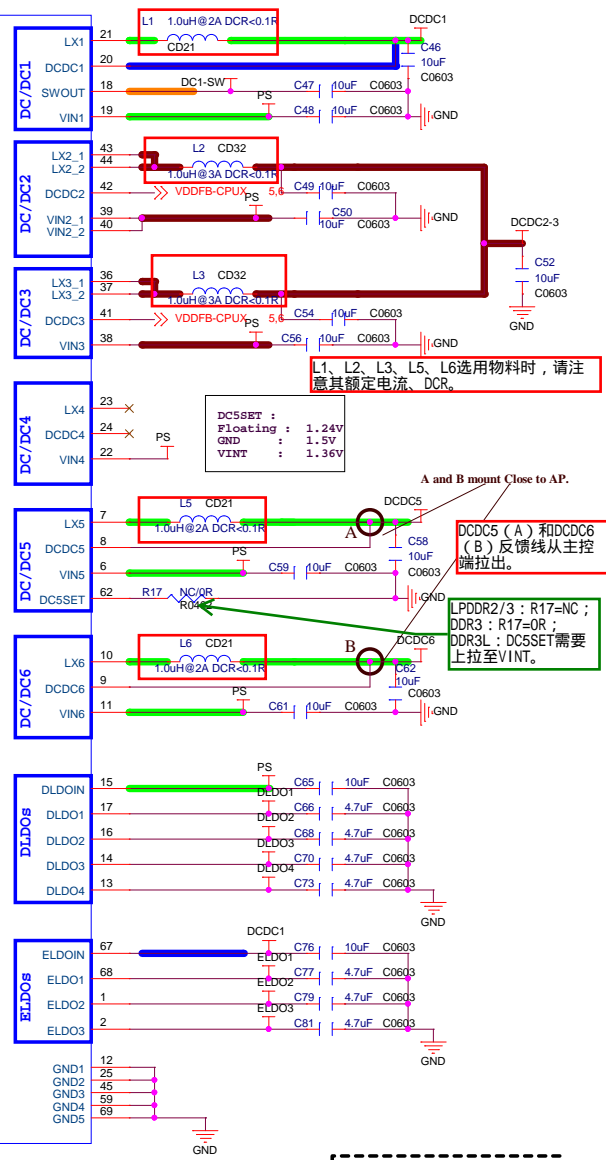
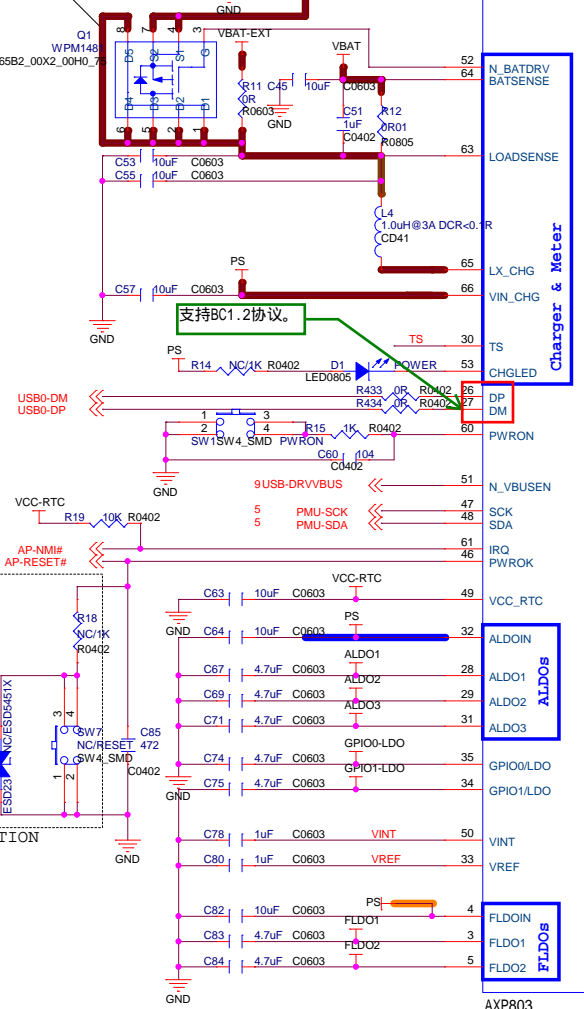
# Power BAT

IF use the battery temperature sensor: A=NC  
otherwise: A=10k

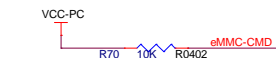


## PMIC

V<sub>th</sub> < 1.5V  
R < 30m ohm  
V<sub>GS</sub> < 4.5V

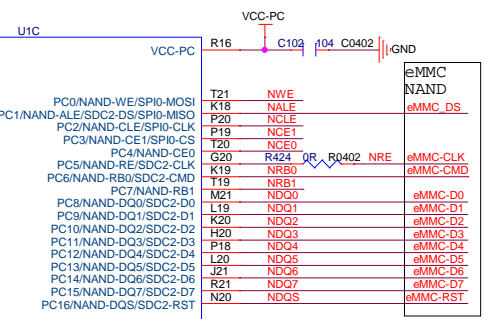


# NAND/eMMC

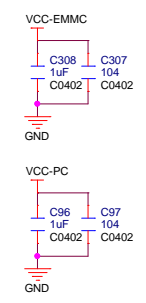
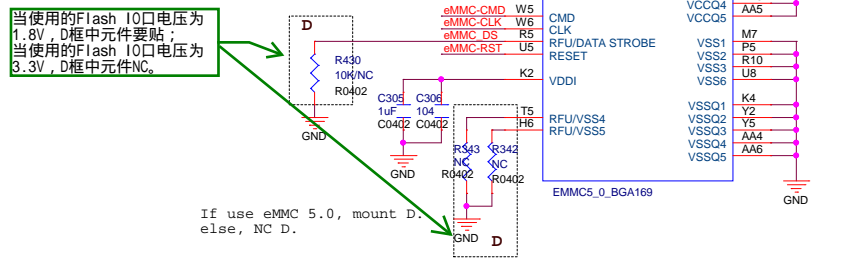


当使用的Flash IO口电压为1.8V，D框中元件要贴；  
当使用的Flash IO口电压为3.3V，D框中元件不贴。

If use eMMC 5.0, mount D.  
else, NC D.



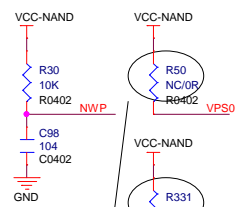
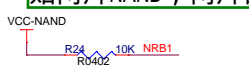
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Both eMMC NAND and first TSOP NAND layout together

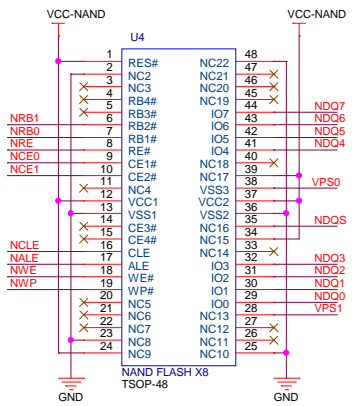
- (1) 1 NAND : [ 1 CE or 2 CE ]
- (2) 2 NAND : [ 1 CE ]

贴一片NAND，可以是1 CE或2 CE；  
贴两片NAND，两片都为1 CE。

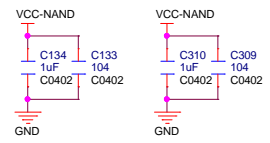
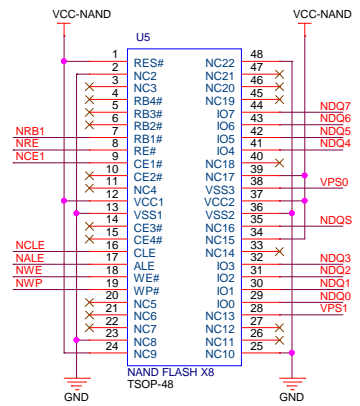


Please mount this two resistors if use Sandisk or Toshiba nand flash

The first NAND FLASH



The second NAND FLASH



# AUDIO

## HP\_JACK

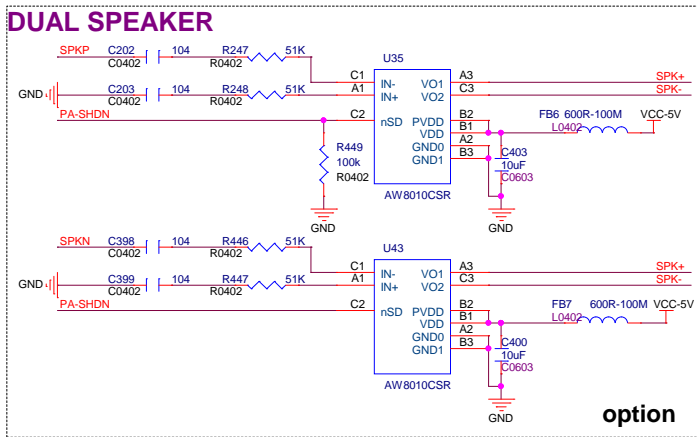
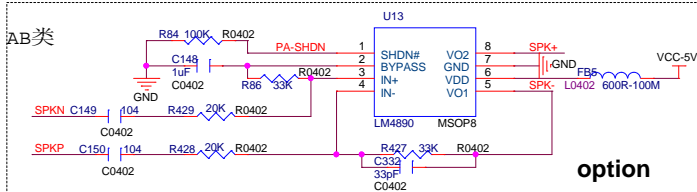
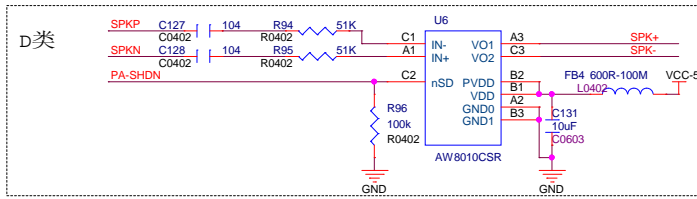
通过判断HP-DET信号是否满足预先设定的阈值，来判断是否有耳机插入！

0伏直驱反馈信号。

R87 47K电阻不能删除！用于保证在耳机插入的情况下能稳定检测到电平！

R88一定要靠近耳机座。

## SPEAKER



## ECM AMIC

注意1：  
不插入耳机，耳机座子4脚与3脚断开；插入耳机，耳机座子4脚与3脚短路；R104 NC不贴！

注意2：  
不插入耳机，耳机座子4脚与3脚短路；插入耳机，耳机座子4脚与3脚断开；R104 贴100K！软件需要调整。

Note1:  
When insert HP, pin4 and pin3 is connected, when pull out HP, pin4 and pin3 is disconnected.

Note2:  
When insert HP, pin4 and pin3 is disconnected, when pull out HP, pin4 and pin3 is connected. Mount R104 100K.

## S AMIC

## MEMS DMIC

## RECEIVER

- 5 MBIAS
- 5 HBIAS
- 5 HP-DET
- 5 HP-OUTL
- 5 HP-OUTR
- 5 MIC2N
- 5 MIC2P
- 5 MIC1N
- 5 MIC1P
- 5 HS-MIC
- 9 DMIC-CLK
- 9 DMIC-DIN
- 5 EAROUTP
- 5 EAROUTN
- 5 LINEOUTP
- 5 LINEOUTN
- 9 PA-SHDN





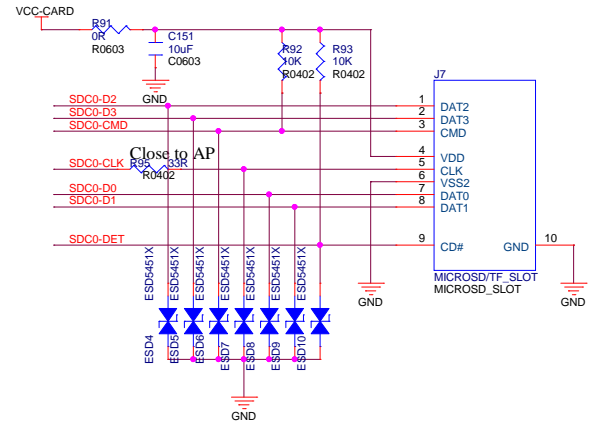
# T-CADD/USB

## T-CARD

U1G

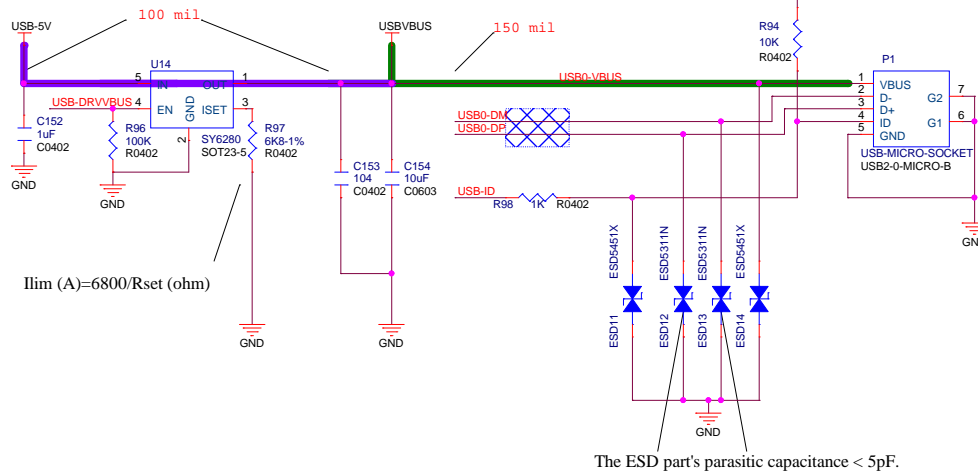
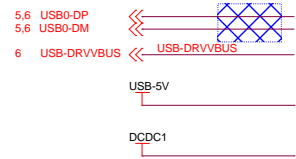
PF0/SDC0-D1/JTAG-MS1	AB10	SDC0-D1	
PF1/SDC0-D0/JTAG-DI1	W13	SDC0-D0	
PF2/SDC0-CLK/UART0-TX	AC8	SDC0-CLK	
PF3/SDC0-CMD/JTAG-DO1	W9	SDC0-CMD	
PF4/SDC0-D3/UART0-RX	AB6	SDC0-D3	
PF5/SDC0-D2/JTAG-CK1	AB9	SDC0-D2	
PF6	AB8	SDC0-DET	
PH0/TWI0-SCK	W11	TWI0-SCK	11
PH1/TWI0-SDA	AA10	TWI0-SDA	11
PH2/TWI1-SCK	AC4	TWI1-SCK	12
PH3/TWI1-SDA	AA9	TWI1-SDA	12
PH4/UART3-TX	AB5	CTP-INT	11
PH5/UART3-RX	AC7	GS-INT	12
PH6/UART3-RTS	AB4	LS-INT	12
PH7/UART3-CTS	AC5	PA-SHDN	8
PH8/SPDIF-OUT	Y10	CTP-RST	11
PH9	AA8	USB-ID	
PH10/MIC-CLK	Y8	DMIC-CLK	8
PH11/MIC-DATA	AA5	DMIC-DIN	8

A64



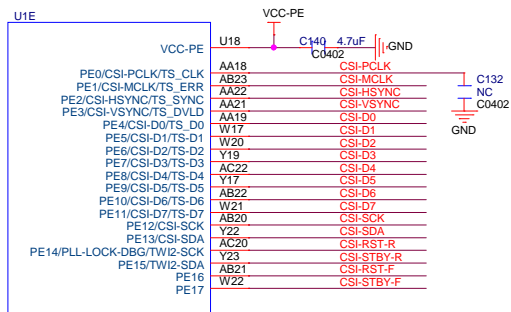
## USB

Differential pairs  
Z0= 90 ohm

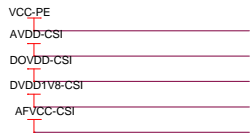


The ESD part's parasitic capacitance < 5pF.

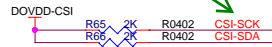
# CAMREA



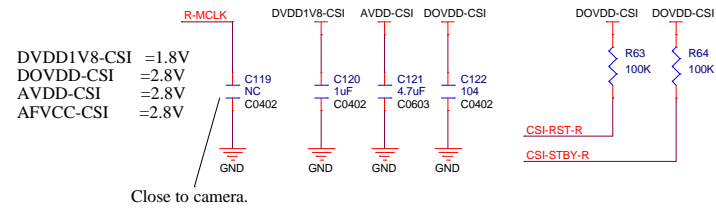
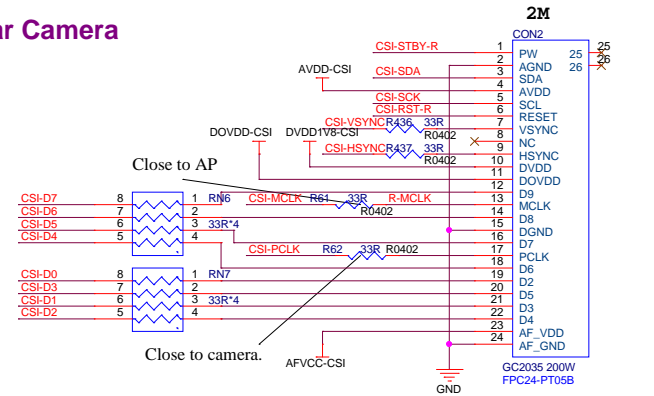
A64



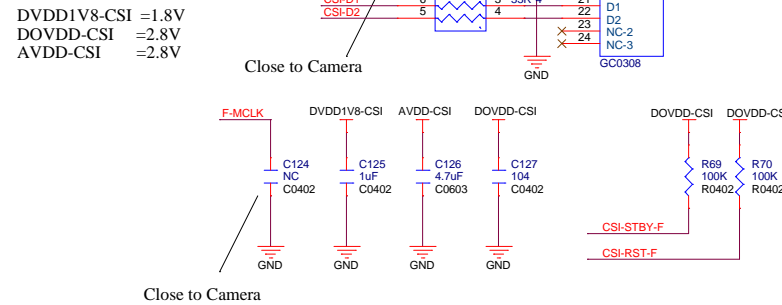
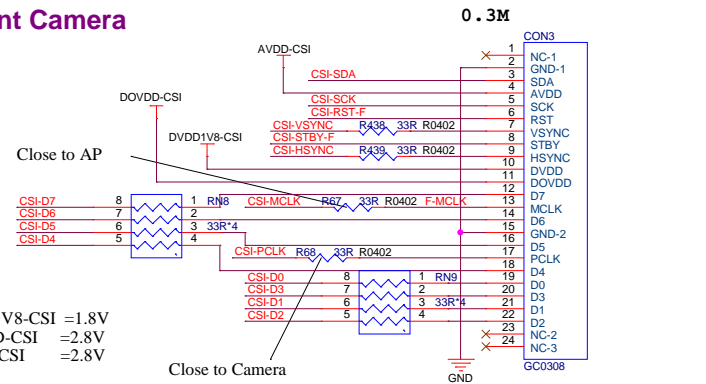
Camera的I2C不要和其它器件复用。



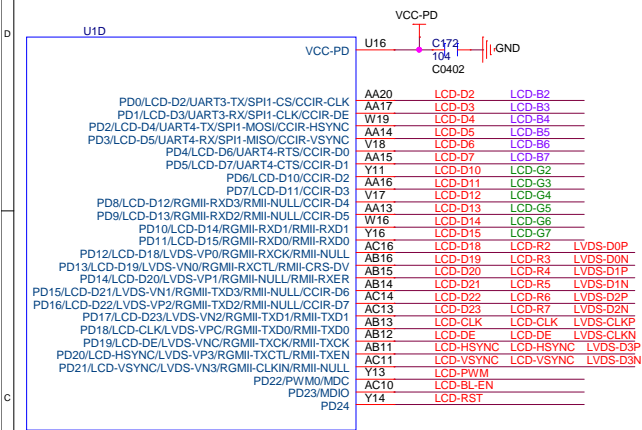
## Rear Camera



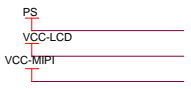
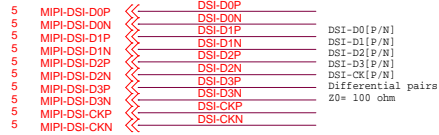
## Front Camera



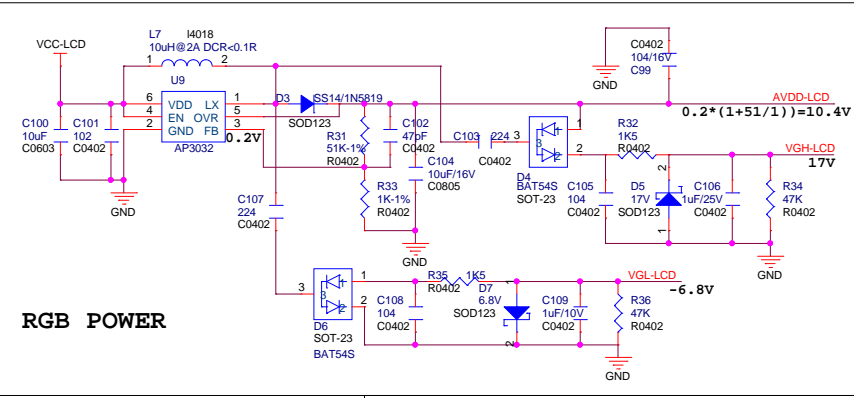
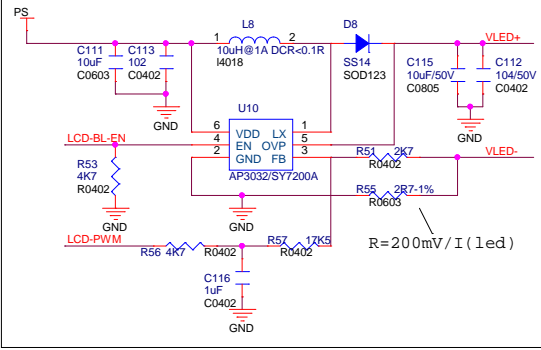
# LCM/CTP



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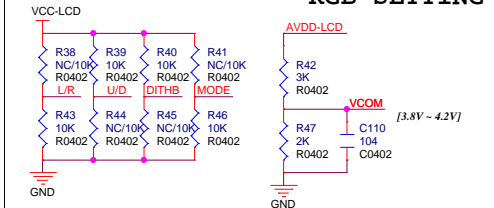


## Backlight

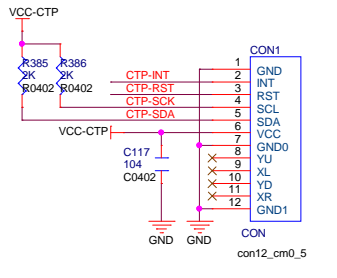


## RGB POWER

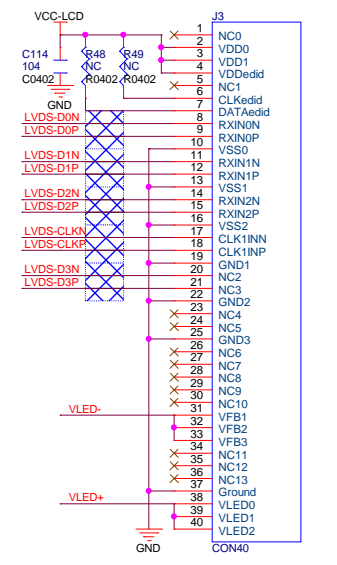
## RGB SETTING



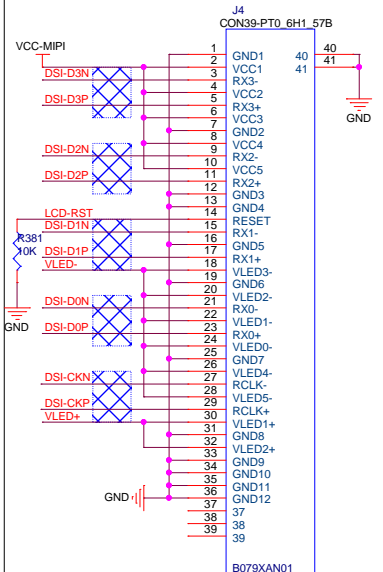
## CTP



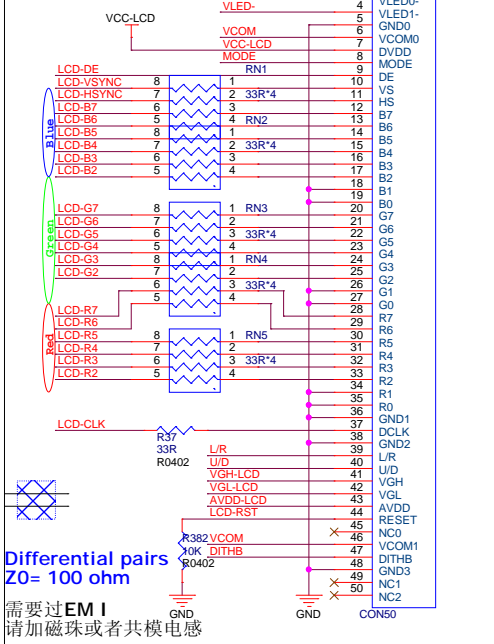
## LVDS



## MIPI



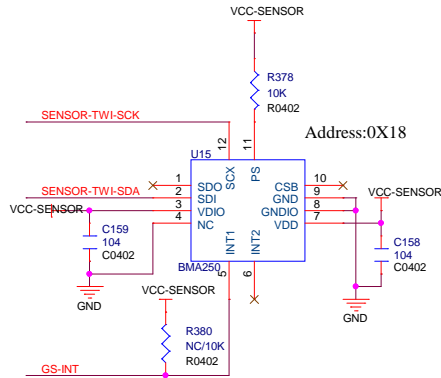
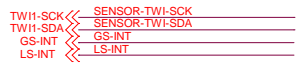
## RGB



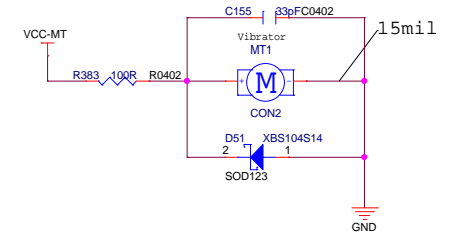
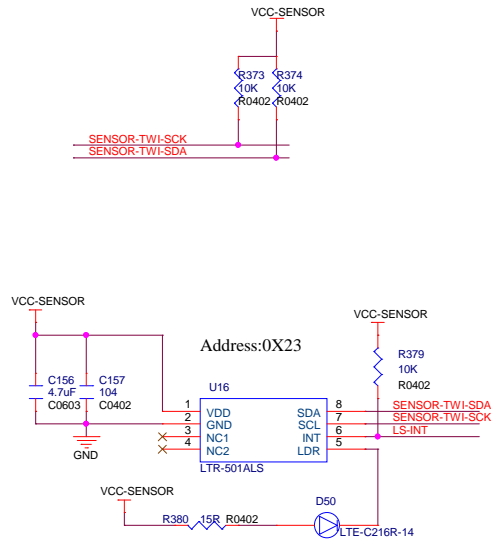
# SENSORs/MT/KEY

## SENSOR

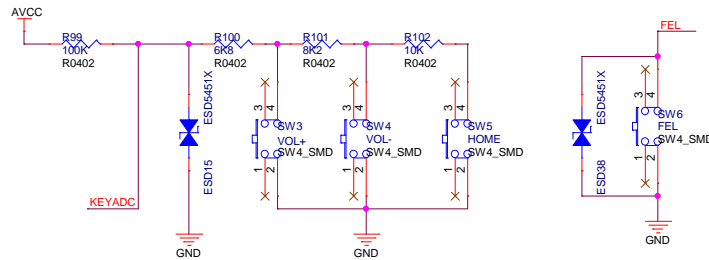
## Motor



place PIN1 in the top right, parallel to the screen, and put on the top left of the screen



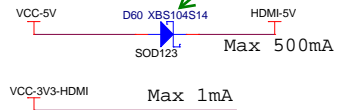
## KEY



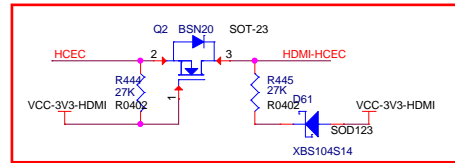
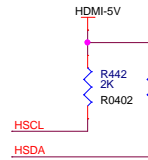
# HDMI



防止接入HDMI时，在系统待机状态下向系统倒灌电。

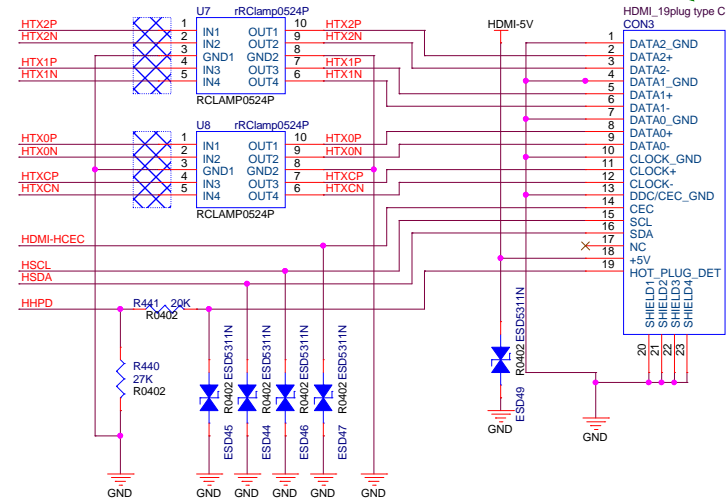


Differential pairs  
Z0= 100 ohm



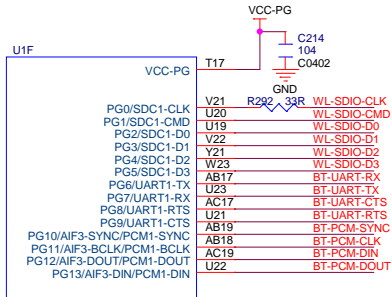
防止接入HDMI时，在系统待机状态下向系统倒灌电；若不需要CEC功能，该电路可不贴，HDMI-HCEC信号悬空。

在做原理图设计时，请注意HDMI座的型号，型号不同，线序不同，请注意！



# WIFI+BT

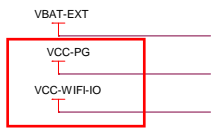
A



A64



3



I/O电压根据模组datasheet进行调整：  
 AP6181: 1.71V-3.6V ;  
 AP6210: 1.71V-3.6V ;  
 8723BS: 1.62V-3.6V ;  
 AP6330: 1.2V-2.9V ;  
 AP6335: 1.71V-3.63V, 若使用802.11ac协议, 必须为1.8V.

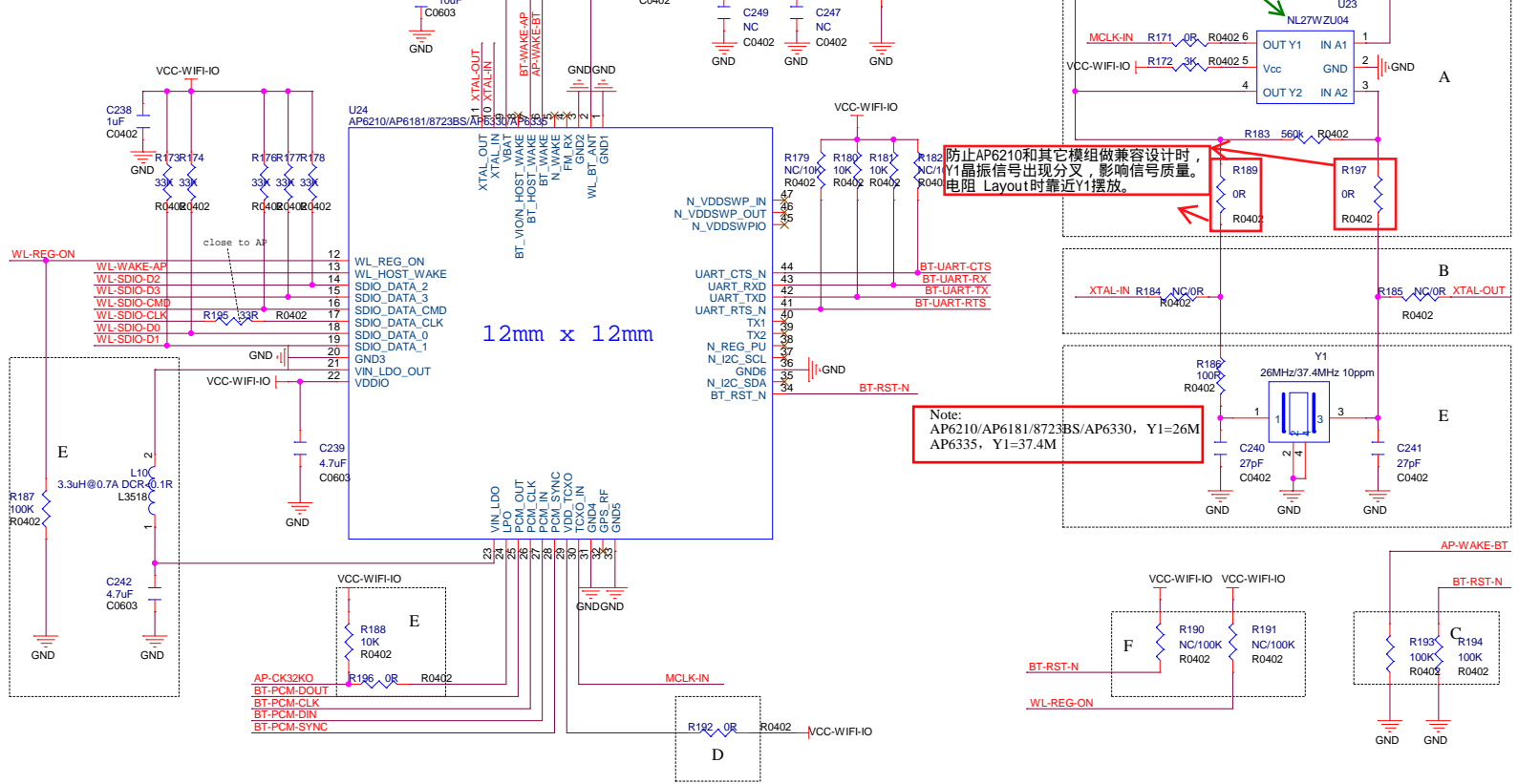
2



1

B

Note:  
 AP6210, Mount A+C+D+E, NC B+F  
 AP6181, Mount B+E, NC A+C+D+F  
 8723BS, Mount F, NC A+B+C+D+E  
 AP6330/6335, Mount B+C+E, NC A+D+F

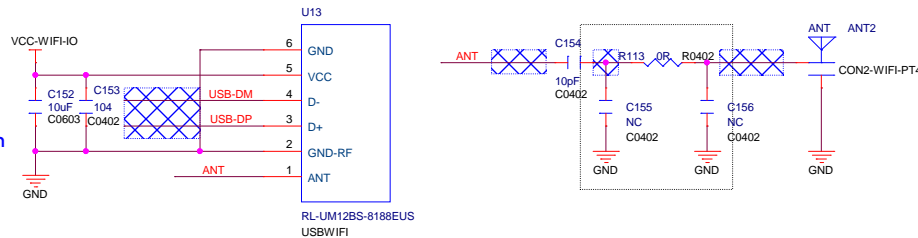


# USB WIFI

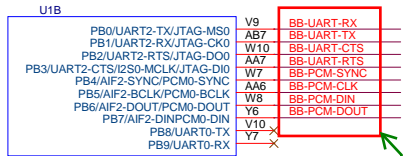
Differential pairs  
 ZO= 90 ohm



50 ohm

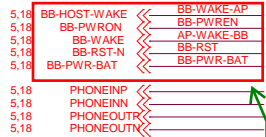


# MODEM-2G



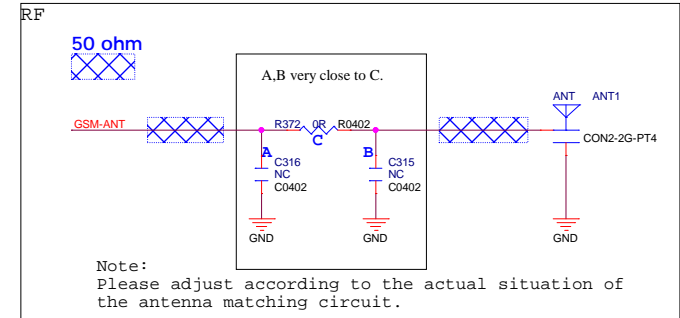
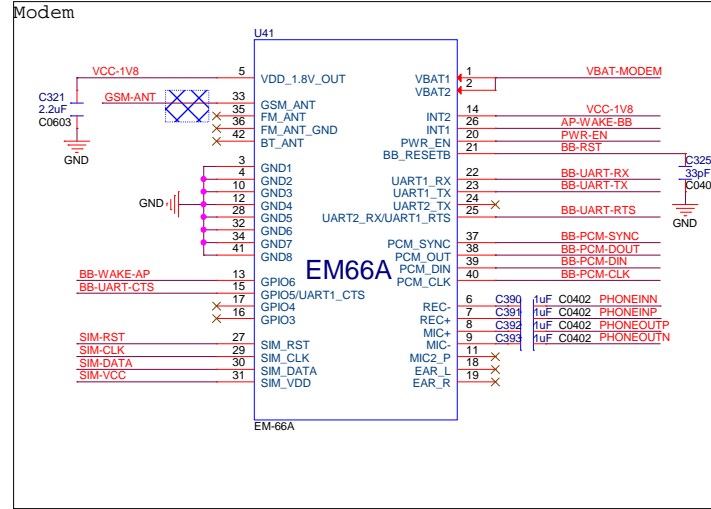
A64

请注意链接关系，输入、输出不要接错！

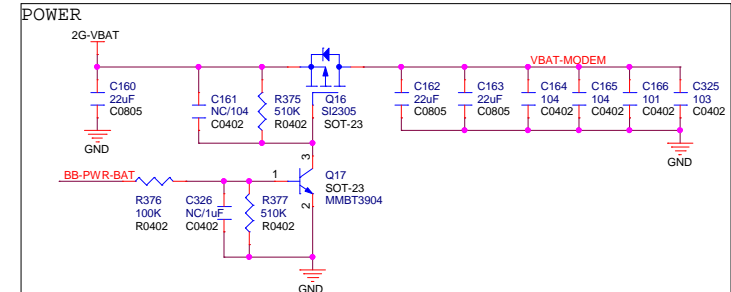
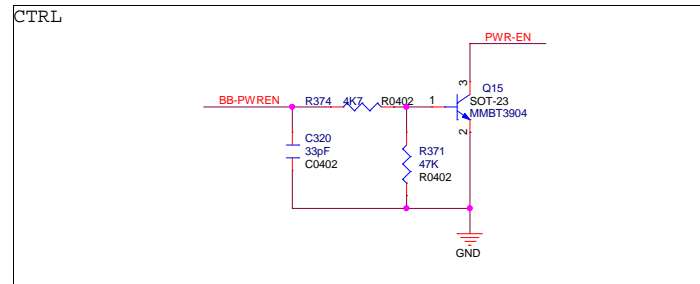
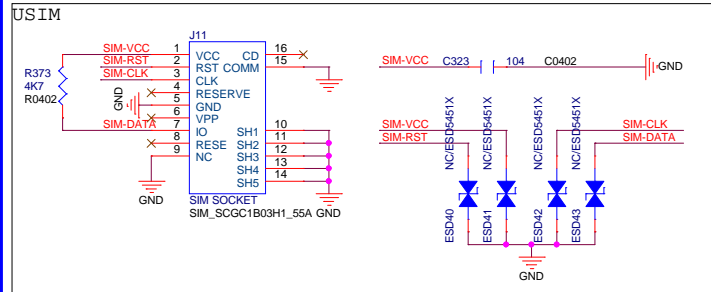


模组IO电压2.8V-3.3V，若VCC-PL电压为1.8V，则需要进行IO电平转换！

2G-VBAT

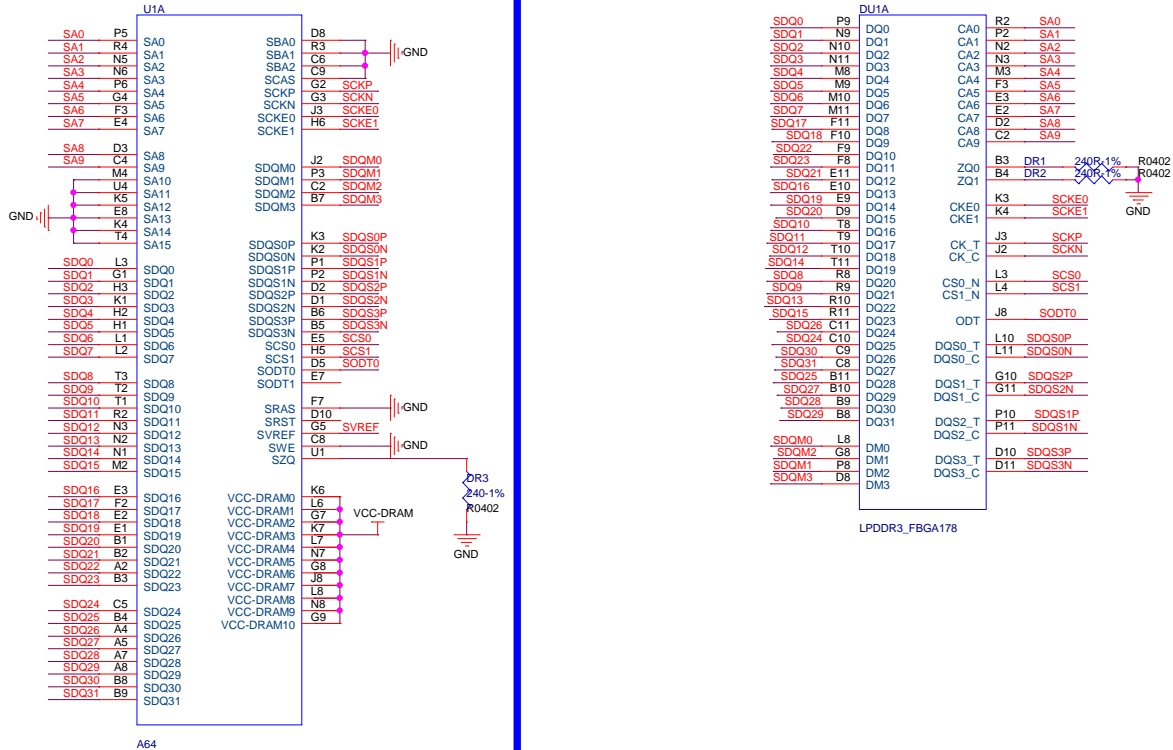


这部分电路根据天线实际情况调整。

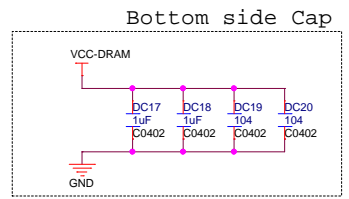
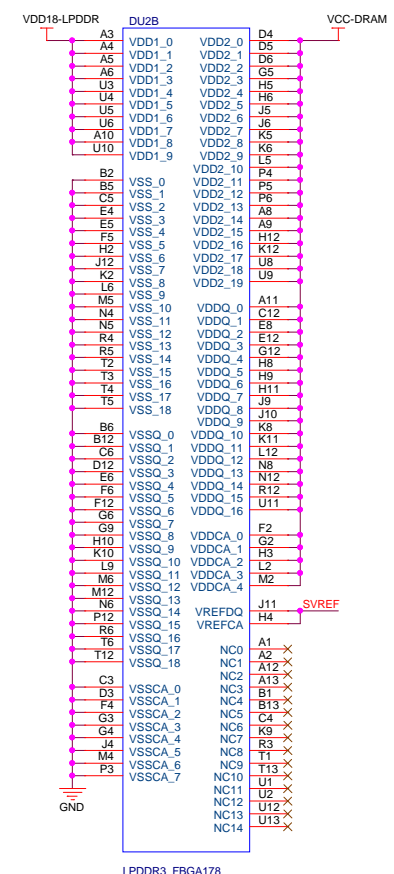
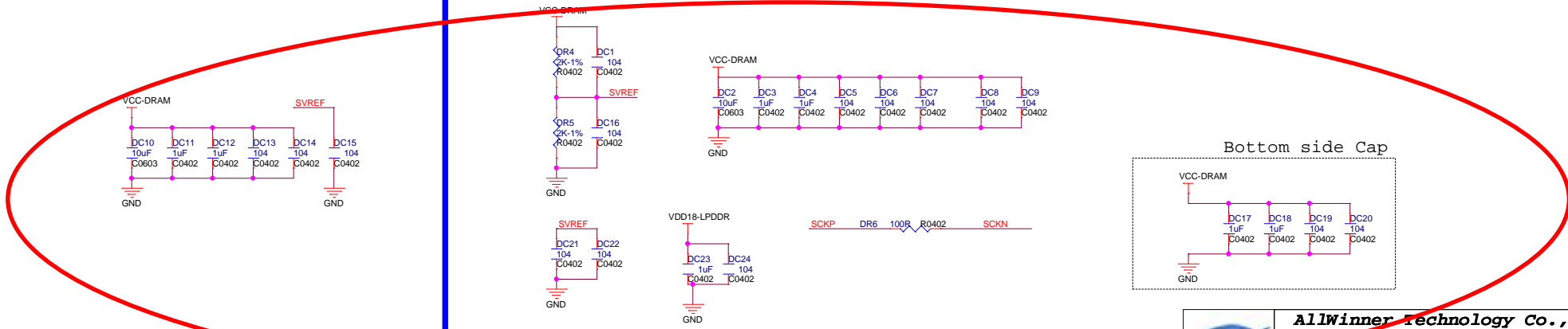


# LPDDR3

请尽量使用Allwinner提供的DDR Layout参考模板；否则请严格遵守DDR Layout Guide。



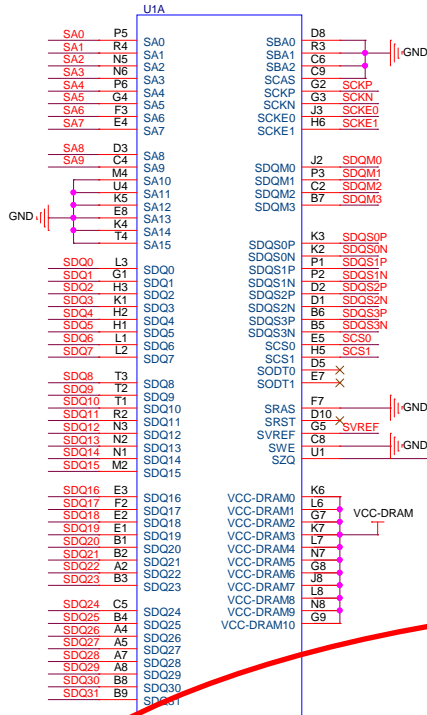
采用Allwinner DDR Layout模板，红色框中的元器件位号不能变。





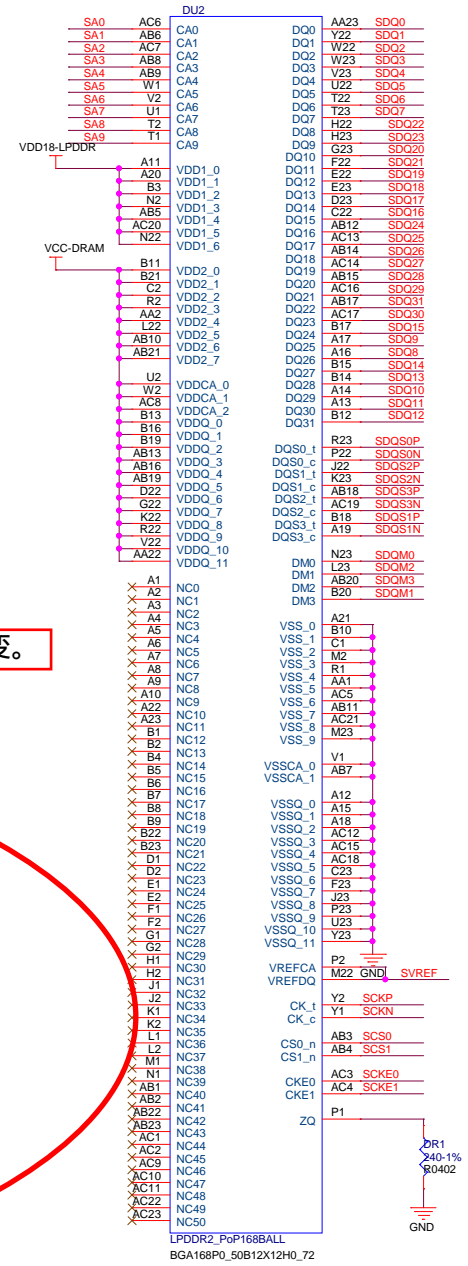
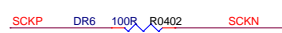
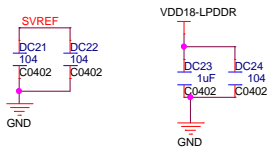
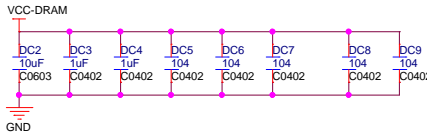
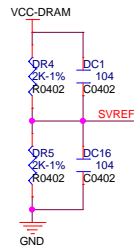
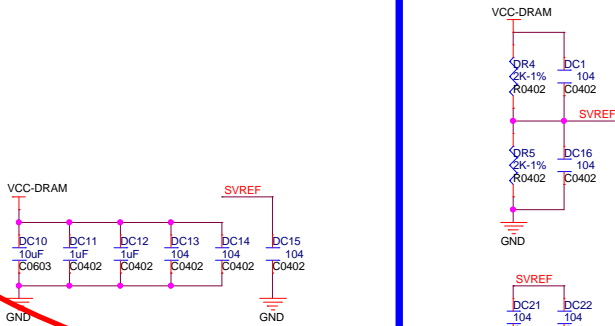
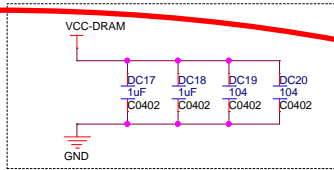
# LPDDR3/LPDDR2

请尽量使用Allwinner提供的DDR Layout参考模板；否则请严格遵守DDR Layout Guide。

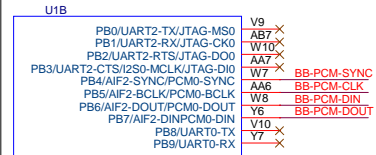


采用Allwinner DDR Layout模板，红色框中的元器件位号不能变。

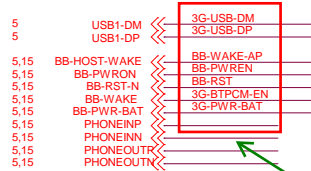
Bottom side Cap



# MODEM 3G



A64

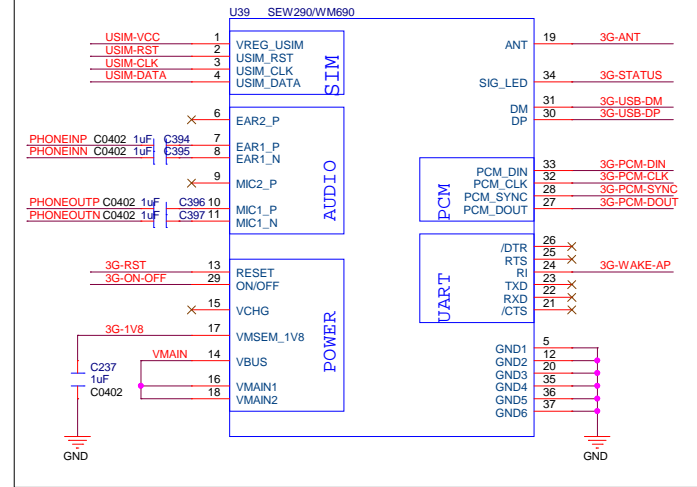


模组IO电压为2.8V~3.3V, 若VCC-PL电压为1.8V, 则需要进行IO电平转换!

3G-VBAT 3.4~4.2V

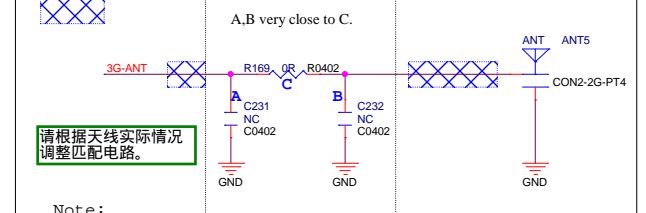
DCDC1

## Modem



RF

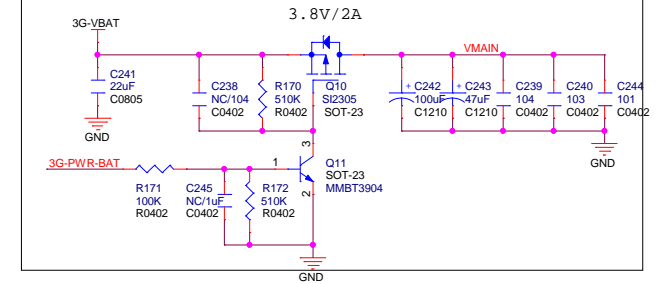
50 ohm



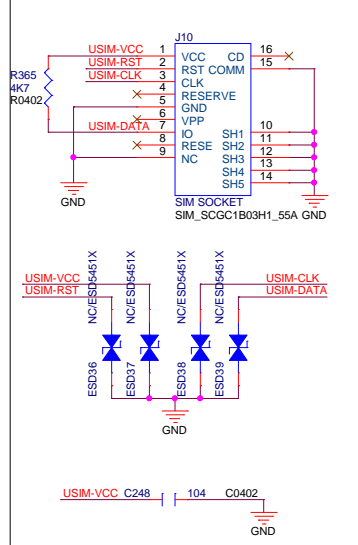
请根据天线实际情况调整匹配电路。

Note: Please adjust according to the actual situation of the antenna matching circuit.

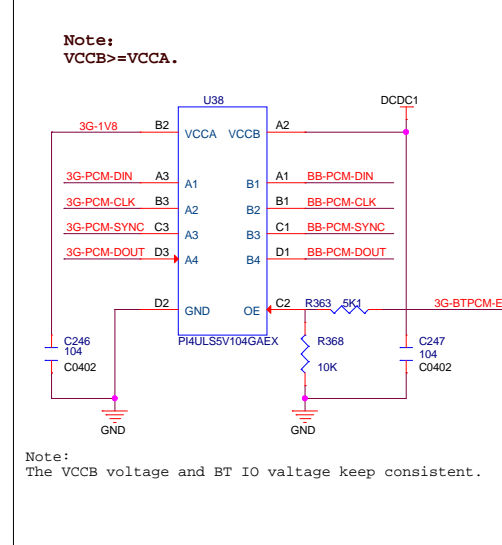
POWER



## USIM



## LEVEL TRANSFORM



## CTRL

